IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re patent application of

Deok-kee Kim et al. Conf. No.: 4565

Serial No.: 10/710,566 Group Art Unit: 2811

Filed: July 21, 2004 Examiner: A. Arena

For: TOP-OXIDE-EARLY PROCESS AND ARRAY TOP OXIDE PLANARIZATION

Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

APPELLANT'S BRIEF UNDER 37 C.F.R. §41.37

This brief is in furtherance of the Notice of Appeal, filed in this case on August 3, 2007, and following a Notice of Panel Decision from Pre-Appeal Brief Review mailed September 17, 2007.

This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. §41.37(c)):

I. REAL PARTY IN INTEREST

II. RELATED APPEALS AND INTERFERENCES

III. STATUS OF CLAIMS

IV. STATUS OF AMENDMENTS

V. SUMMARY OF CLAIMED SUBJECT MATTER

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

VII. ARGUMENTS

- ☐ ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH
- ☐ ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH
- ☑ ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102
- ☑ ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103
- ☐ ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

VIII. CLAIMS APPENDIX

IX. EVIDENCE APPENDIX

X. RELATED PROCEEDINGS APPENDIX

I. Real Party in Interest

The real party in interest in the appeal is:

☐ the party named in the caption of this brief.

☑ the following party:

International Business Machines Corporation of Armonk, New York

II. RELATED APPEALS AND INTERFERENCES

With respect to other appeals, interferences or judicial proceedings that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal:

☑ there are no related appeals, interferences or judicial proceedings related to, which directly affect or may be directly affected by or have a bearing on the Board's decision in this pending Appeal.

☐ these are as follows:

III. STATUS OF CLAIMS

The status of the claims in this application are:

A. Total number of claims in Application

Claims in the application are: Claims 1 - 20

B. Status of all the claims:

1. Claims cancelled: None
2. Claims withdrawn from consideration but not cancelled: None
3. Claims pending: Claims 1 - 20
4. Claims allowed: None
5. Claims rejected: Claims 1 - 20

C. Claims on Appeal.

The claims on appeal are: Claims 1 - 20

IV. STATUS OF AMENDMENTS

The status of amendments filed subsequent to the final rejection are as follows:

No amendments to the application have been filed subsequent to the final action of April 3, 2007. The response to that final action, which did not present any amendments, has been entered and considered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention as defined in the claims on appeal is directed to the formation and protection (during other wafer/chip processing) of a structure in the form of a patterned layer of isolation material extending over particular circuit elements which, at the present state of the art, is required in virtually all integrated circuits having differentiated circuit areas and which are formed at high integration density such that closely spaced connections must be formed over layers containing circuit elements (which have different structures in the respective differentiated areas, see ¶ 0003); thus requiring an isolation layer (see ¶ 0004) to be formed over the circuit elements in at least one of the differentiated circuit areas on or in which the closely spaced connections are formed. A particularly demanding and critical high density integrated circuit having differentiated circuit areas is a memory chip having differentiated array and support areas and in which the isolation material layer structure is an isolation material layer is referred to as an array top oxide (ATO), as recited in original claim 2 and discussed, for example, in ¶ 0004. The invention is thus disclosed in connection with such a memory structure (while not limited thereto) in which the formation of the required array top oxide is particularly difficult and critical, particularly in regard to manufacturing yield, but is also applicable to many other types of integrated circuits such as a processor or logic array having an embedded memory.

The principal reason for such criticality, particularly in memory chips, is the need for a high degree of planarity of the surface of the isolation layer or ATO in order to support sufficient resolution of lithographic patterning to form the connections which must usually be narrow and in close proximity to each other. For current and foreseeable integrated circuit designs, a planarity tolerance of 15 nm is needed, which cannot be reliably met by known processes and integrated circuit structures prior to the invention. Prior to the invention, planarization was typically performed by polishing processes such as chemical-mechanical polishing (CMP).

However, polishing processes may cause defects or artifacts such as scratching or chipping (one often aggravating the other). Polishing processes are also subject to "dishing" in large areas having low surface hardness (e.g. where polish stops are not or cannot be provided within the large area) or where large changes in surface height between differentiated areas of a chip are presented by the surface to be planarized (see also, for example, ¶ 0034). Such dishing greatly compromises the ability to meet the needed 15 nm planarity tolerance to support lithographic patterning of connections, as alluded to above. Further, the isolation layer or ATO is also subject to damage from other semiconductor fabrication processes as well as from chipping and scratching during the planarization process. The known techniques of fabrication of an isolation layer or ATO, known as top oxide early (TOE), top oxide-nitride (TON) and top oxide late (TOL), as summarized in ¶ 0005, each have particular disadvantages in regard to susceptibility of the ATO to particular types of damage, as also summarized in ¶ 0005 as well as ¶0008 and noted elsewhere in connection with particular ATO formation techniques such as at ¶ 0034. For purposes of disclosure of the invention, three embodiments or variants of the invention are respectively disclosed employing each of the three known techniques of ATO formation (e.g. the first embodiment is disclosed in connection with a TOE process, the second embodiment is disclosed in connection with a TON process and the third embodiment is disclosed in connection with a TOL process) although each of the three embodiments can be used in connection with any of the known ATO formation processes. The three embodiments of the invention are summarized in ¶0026.

The inventors have discovered that the frequency of damage due to scratching and chipping and the like during planarization by polishing processes varies with the amount of material removed during planarization by polishing and that the amount of material that must be removed by planarization can be decreased (with a corresponding reduction in the frequency of such defects) by deglazing to reduce the

step height (defined in ¶ 0050) of structures such as isolation trenches (ITs) in the areas where the ATO is to be formed. (In the case of reduction of height of isolation trenches and the like to reduce step height, for example, the height of isolation trenches is restored/replaced by the ATO; thus representing material which is not removed by polishing.) This feature is of general applicability and preferably used in each of the three exemplary disclosed embodiments of the invention and is a principal claimed characteristic or feature of the first embodiment of the invention in generic independent claim 1 and claims 2 - 7, depending therefrom. Particular devices to which the first embodiment is preferably applied are recited in dependent claims 9 and 10.

The second embodiment of the invention involves, as illustrated in Figures 1 and 10 - 14 and described beginning at ¶0033, a technique of planarization capable of meeting a 15 nm planarity tolerance which avoids polishing processes and the resultant scratching and/or chipping (which is minimized but not necessarily eliminated by the first embodiment) altogether (see ¶¶ 0034 and 0035). This planarization technique involves application of a resist, anti-reflection coating (ARC), spin-on glass (SOG) or the like (exemplary suitable materials are discussed in ¶ 0036) which forms a highly planar surface and performing a non-selective etching from that highly planar surface. Suitable etching conditions and etchants to achieve a sufficient degree of non-selectivity of the etching process are also discussed in ¶0036. The planarization technique of the second embodiment of the invention is also of general applicability (see ¶0038) and is enhanced by use in combination with the step height limitation technique of the first embodiment since the reduction of amount of material removed reduces the effects of any small degree of non-selectivity of the etch that is not avoided (e.g. by slight excess of oxygen or nitrogen during etching as discussed in ¶ 0036) by maintaining suitable etching conditions. The second embodiment of the invention is separately claimed in independent claims 12 and 16 and dependent claims

13 (directed to the additional step of end-point detection for the etching process as discussed at ¶¶ 0036, 0042 and 0044) and 15 and, in combination with the first embodiment in dependent claims 11 and 20 with applications to TOE, TON and TOL. processes being recited in clams 17 - 19, respectively.

The third embodiment of the invention, illustrated in Figures 15 - 22 and discussed beginning at ¶ 0048, involves removal of an impediment to developing a suitably planar surface with a resist, ARC, spin-on glass or the like in accordance with the second embodiment of the invention. Specifically, as discussed at ¶¶ 0046 and 0047, differentiated areas of a chip or wafer having significantly increased height (as distinct from step height within particular areas or across the chip or wafer) will cause an excess of the planarizing material (e.g. the resist, ARC, spin-on glass, etc.) near the boundaries of the areas of increased height, as illustrated in Figure 18, and discussed at ¶0051, causing so-called picture frame defects and contamination due to material being undercut by etching and thus developing particles which can remain on the chip (in much the same manner that material abraded by polishing or chipping can remain on the chip or, perhaps more importantly, contribute to additional scratching and/or chipping). The third embodiment of the invention avoids such problems by equalizing average heights (as distinct from step heights) of respective differentiated areas. The third embodiment is also of general applicability but is preferably employed prior to planarization in accordance with the second embodiment and is so claimed in independent claim 14 and dependent claims 15. It is also claimed in combination with the first embodiment in dependent claim 8.

In summary, specific support for particular elements or steps recited in the claims on Appeal can be found in the original specification and drawings in at least the following locations, as indicated in tabular form. However, it is to be understood that the invention and its particular exemplary embodiments and usage with known exemplary processes are disclosed throughout the application as originally filed and

that the context of the locations indicated below as well as combinations of usages indicated in the specification should be fully considered to obtain an understanding of the nature of the invention, particularly in its various embodiments and applications.

1. A method for manufacture of an integrated circuit having structures formed in respective first and second areas thereon, said method comprising steps of	¶¶ 0003 - 0008
reducing height of structures in said first and second areas to control step height in said first and second areas,	Figures 3, 10 and 15, ¶¶ 0015 and 0026
removing a material from said first and second areas simultaneously or sequentially, and replacing said material removed from said first and second areas with a first material in said first area and a second material in said second area, respectively, one of said first and second materials being an isolation material,	For example, removal of hard mask 36 (and optional support liner 34) sequentially in respective areas as Figures 4 and 8, see ¶¶ 0028 and 0031 For example, gate poly 90 in support area (Figure 9) and isolation material/ATO in array area (Figure 5)
using a polysilicon block-out mask or a block-out mask having two layers of different materials to protect one of said first and second areas to separately process the other of said first and second areas,	See ¶¶ 0015, 0027, Figure 4, also Figures 7, 8, 14B and 19; ¶¶ 0031, 0037 and 0054
planarizing said first and second materials to provide a planar surface, and	Figures 6, 13 - 14A and 17 and 19, respectively

(Claim 1 cont'd) completing said integrated circuit.	BEOL processes such as for forming word lines and bit lines, see, for example, ¶ 0031
2. The method as recited in claim 1, wherein said isolation material is an array top oxide.	As above ¶ 0004
3. The method as recited in claim 1, wherein a polysilicon hard mask is used to mask said second area.	As above Figure 3, see ¶ 0015, Figures 7, 8, 14B and 19 as discussed above
4. The method as recited in claim 3, wherein said polysilicon hard mask comprises a single layer of polysilicon.	As above, see, especially ¶0015
5. The method as recited in claim 1, wherein a polysilicon hard mask is used to mask said first area.	As above For example, Figure 8 as discussed above
6. The method as recited in claim 5, wherein said polysilicon hard mask comprises a single layer of polysilicon.	As above, see, especially, ¶ 0015
7. The method as recited in claim 1, including the further step of depositing a nitride liner prior to said step of depositing said isolation material.	As above For example, nitride liner 54, Figure 5, ¶ 0029

8. The method as recited in claim 1, including the further step of equalizing heights of structures in said first and second areas by etching prior to said planarizing step.	As above Third embodiment in combination with first embodiment, Figure 16 (cf. Figure 18), ¶¶ 0050 - 0051
9. The method as recited in claim 1, wherein said integrated circuit is a memory device, said first area is a memory array area and said second area is a support area.	As above All Figures (exemplary application), see ¶ 0024
10. The method as recited in claim 1, wherein said integrated circuit includes an embedded memory, said first area is a memory array area and said second area is a support area.	As above All Figures (alternative exemplary application), see ¶ 0024
11. The method as recited in claim 1, wherein said planarizing step includes applying a planarizing material over said structures in said first and second areas and said first and second materials, and non-selectively etching said planarizing material, said first material, said second material and said structures.	As above (combination of first and second embodiments) Figure 13, ¶ 0035 Figure 14A, ¶0036

12. A method for planarizing a surface having structures formed thereon and an additional layer of material covering said surface and said structures formed on said surface, said method including steps of	Second embodiment, *per se* - Figures 10 - 14B, description beginning at ¶ 0033
applying a planarizing material to said additional layer of material to form a substantially planar surface above said surface having structures formed thereon, and	Figure 13, ¶0035
performing a non-selective etching from said substantially planar surface to a said structure formed thereon.	Figure 14A, ¶ 0036

13. The method as recited in claim 12, including the further step of	As above
performing end point detection to detect a material interface for determining termination of said step of non-selective etching.	Figures 14A, 15G, see ¶ 0042

14. A method as recited in claim 12, wherein	As above
said structures have a first average height in a first area of said surface and structures of a second average height greater than said first average height in a second area of said surface, said method comprising the further steps of	Figures 5 and 18, see ¶¶ 0045 - 0051 (Conditions favoring supplementing the second embodiment with the third embodiment)
etching said structures of said second average height to an average height substantially equal to said first average height,	Figure 16, ¶ 0050 (third embodiment)
subsequent to said etching step, applying a planarizing material to said first and second areas of said surface and covering said structures remaining in said first and second areas whereby a surface of said planarizing material is substantially planar, and	Figure 17, ¶ 0051
performing said step of non-selectively etching said planarizing material and structures overlaid by said planarizing material to completely remove said planarizing material and form a planar surface.	As above

15. The method as recited in claim 12, wherein said step of non-selective etching includes removal of a nitride liner below said layer of material.	As above Figure 14B, ¶0037
16. A method for planarizing a surface of a body of material, said method including steps of applying a planarizing material to said body of material to form a substantially planar surface, and performing a non-selective etching from said substantially planar surface to a point on or within said body of material.	Second embodiment *per se* as applied to a generalized surface - Figures 10 - 14B, description beginning at ¶ 0033 Figure 13, ¶ 0035 Figure 14A, ¶ 0036
17. The method as recited in claim 16 in combination with a top oxide early process for forming an integrated circuit.	As above See ¶ 0038
18. The method as recited in claim 16 in combination with a top oxide nitride process for forming an integrated circuit.	As above Exemplary application of second embodiment - Figures 10 - 14B, description beginning at ¶ 0033

19. The method as recited in claim 16 in combination with a top oxide late process for forming an integrated circuit.	As above See ¶ 0038

20. The method as recited in claim 16 including the further step of adjusting height of a structure on a differentiated area of said body of material.	As above Addition of third embodiment to generalized second embodiment - Figures 15 - 22, see ¶¶ 0041 and 0049

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The grounds of rejection to be reviewed on Appeal are:

1. The rejection of claims 1 - 4, 7 - 12 and 14 - 20 under 35 U.S.C. §102 as being anticipated by Hummler;

2. The rejection of claims 5 - 6 under 35 U.S.C. §103 as being unpatentable over Hummler; and

3. The rejection of claim 13 under 35 U.S.C. §103 as being unpatentable over Hummler in view of Gustafson et al.

ARGUMENT VIIA. REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, first paragraph.

ARGUMENT VIIB. REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

There are no grounds of rejection under 35 U.S.C. §112, second paragraph.

ARGUMENT VIIC. REJECTIONS UNDER 35 U.S.C. §102

Introduction

Claims 1 - 4, 7 - 12 and 14 - 20 stand rejected under 35 U.S.C. §102 as being anticipated by Hummler (6.620,677). This ground of rejection has been traversed as being *prima facie* in error since the Examiner has admitted in regard to claim 1 that certain claim recitations have been given no weight and essentially ignored while substantially admitting that Hummler does not contain teachings which answer such recitations. In regard to other claims, such as claims 12, 14 and 16, the Examiner's assertions in regard to the teachings of Hummler are respectfully submitted to be not well-supported by the actual content thereof. It is believed important to note in this regard, that Hummler is cited and incorporated by reference in paragraph 0015 of the present application as teaching an exemplary top oxide early (TOE) process using a nitride liner over which the present invention provides a significant improvement in protecting differentiated areas of a semiconductor device during manufacture and planarization of the array top oxide (ATO). The failure of the Examiner to accord patentable weight to some recitations and/or construing Hummler through hindsight beyond the actual content thereof, the Examiner has effectively refused to consider the very features of the invention which provide and support its meritorious effects which are not available from Hummler.

Claims 1 - 4 and 7 - 11

In regard to claim 1, the Examiner reads the recitation of reducing height of structures in first and second areas (e.g. deglazing) to control step height, which is indicated to be a significant improvement over Hummler, facilitating planarization, in the same paragraph (¶ 0015) in which Hummler is incorporated by reference on (for the array area 16) the anisotropic etching of layer 46 (deposited to fill divot 37 which is formed as an incident of removing pad nitride) to form spacer 48 as illustrated in

Figures 7A, 7B and 8 and discussed in column 6, lines 40 - 65, *which is silent as to control of step height*, and (for the support area 18) the (explicitly *optional* - column 5, line 57, see also column 7, lines 35+, where the STI is not recessed in the second embodiment of the invention) recessing of STI 38 from surface 39 to surface 40 by an amount approximating half the thickness of pad nitride layer 14 or about 100 to 400 Angstroms as illustrated in Figures 1A and 2A (discussed at column 5, lines 48 - 65) such that portions of both insulating material 52 and liner 54 may be accommodated therein to provide increased process margins and to avoid further recess of the STI by unintended etching, as illustrated in Figure 10 and discussed at column 7, lines 18 - 34, *again without reference to control of step height.* It is clear from the illustration of these features in Hummler, as well as the discussion thereof, that neither has anything to do with control of step height: the anisotropic etching of layer 46/48 leaving step height unchanged and the *filling* of divot 37 is not well-described as *reducing* the height of any structure while recessing of STI 38 appears to *introduce* steps into the support area 18.

The Examiner parenthetically remarks (page 2, lines 10 - 11 of the final rejection of April 3, 2007) that "the recited purpose does (sic) limit the scope of the claims since it does not require any non-recited steps, see MPEP §2111.04". Thus, if the Examiner's comment is taken literally and the recited purpose of controlling step height has been considered, it is respectfully submitted that the Examiner is mistaken since no such purpose but, rather contrary purposes requiring different height reductions, if any, (e.g. the structure in the array area as discussed above merely replaces a spacer without any overall effect on height or step height) are disclosed by Hummler. On the other hand, if the Examiner intended to indicate that the recited purpose does *not* limit the scope of the claim (as appears to be the case, since, otherwise, the Examiner's comment would be unnecessary) , such a position is contrary to anticipation under 35 U.S.C. §102 since it effectively ignores explicit

recitations of the claims which do, in fact, require the height reduction to be performed in a particular manner to answer that explicitly recited purpose.

In regard to claims 3 and 4 (as well as claims 5 and 6, discussed below) while Hummler describes use of a polysilicon hard mask *in combination with* a nitride liner for protection of a second area while processing the first area, it is respectfully pointed out that the first and second areas are not identified as any particular type of area (as they are in claim 9) in claim 1 or 3 - 6 and the basic thrust of claims 3 - 6 is to define the invention by providing for *either* area or both areas to be protected using a polysilicon hard mask alone (e.g. without a nitride liner) which Hummler clearly does not teach, as admitted by the Examiner in the rejection of claims 5 and 6.

With regard to claim 8, which recites an additional step of equalizing heights (as distinct from step heights) of structures, the Examiner merely makes parenthetical mention of structures 48, 34 and 38 by reference number and without reference to any portion of the Hummler disclosure. As can be seen from, for example, Figure 9 of Hummler, the structures called out by the Examiner are of very different heights and the average heights in respective areas are also very different. Therefore, the Examiner has not *prima facie* shown the additional recitations of claim 8 to be answered by Hummler.

Further, claim 11 further defines the *planarizing* step of claim 1 to include application of a planarizing material over the first and second areas followed by a non-selective etching step. As the Examiner correctly points out, Hummler discloses the application of a planarizing material followed by etching at column 7, lines 3 - 17. However, this process is disclosed in Hummler to be for the purpose of removing insulating material 50 from the gate electrode contacts 34 and *no mention is made of the etch being non-selective or that a substantially planar surface is sought as a result of such a process*. Further, there is no enabling disclosure in Hummler of how the etching process could be made sufficiently non-selective to obtain a sufficiently

planar surface (compare the passage of Hummler relied upon by the Examiner with the disclosed particulars and criticalities of obtaining a sufficiently non-selective etching process at ¶0053) if, in fact, one wished to do so while practicing the invention in accordance with Hummler and which Hummler does not even suggest to be desirable, much less obtainable through the process contemplated by Hummler. Therefore, it is clearly seen that Hummler does not, in fact, answer the recitations of claim 11 and, moreover, the Examiner infers such a teaching, not contained in Hummler, through impermissible hindsight.

Claims 12 and 16 - 20

Claims 12 and 16 present the steps recited in claim 11, discussed above, as a "stand-alone" planarization process. Claims 12 and 16 differ by the point to which etching is performed.) As discussed above, while Hummler describes etching from a surface of an applied planarizing material followed by etching, Hummler does not disclose that planarization can be obtained by such a process or provide enabling disclosure of how the etch can be made sufficiently non-selective to obtain planarization. Again, the inferences of such disclosure, which Hummler clearly does not provide, can only be derived through hindsight. Therefore, it is respectfully submitted that Hummler cannot be properly considered to anticipate claim 12 or claim 16.

Claims 18 and 19 depend from claim 16 and recite the process of claim 16 in combination with a top oxide nitride (TON) process and a top oxide late (TOL) process respectively. Since the disclosure of Hummler is limited to an exemplary top oxide *early* (TOE) process, Hummler cannot answer the additional recitations of claims 18 and 19. Further, claim 20 recites the additional step of adjusting height of a structure (e.g. for adjusting step height or average height) in one of the differentiated areas in combination with the planarizing process of claim 16. As previously pointed

out in regard to claims 1 and 8, Hummler does not contain such a teaching while the Examiner merely makes reference to the structures mentioned in the rejection of those claims. Accordingly, it is respectfully submitted that the additional recitations of claims 18 - 20 are not anticipated by Hummler and have not been *prima facie* demonstrated to be unpatentable for that reason, in addition to the Examiner's failure to *prima facie* demonstrate anticipation of claim 16.

Claims 14 - 15

Claim 14 recites etching surface of a second average height (in one area) to an average height substantially equal to a first average height of structures in another area followed by application of a planarizing material and performing a non-selective etching in the manner recited in claims 11 and 12, as discussed above. In the final action of April 3, 2007, the Examiner does not indicate any portion of Hummler that is asserted to teach or even arguably illustrate the etching to reduce the second average height to a height substantially equal to a first average height but rather, asserts that the claim is interpreted such that "substantially equal" includes "slightly greater". On the contrary, a substantial height difference of structures below the ATO is evident in both embodiments of the invention a illustrated in Figure 9 and Figures 10A - 19B, respectively. Clearly, the Examiner has not demonstrated that Hummler answers this recitation of claim 14 and has clearly relied upon impermissible hindsight in asserting that Hummler contains any such teaching. Further, as discussed above, the combination of the remaining steps recited in claim 14, particularly including the non-selective etch from a planar surface for achieving planarization is not taught (or suggested) in Hummler but similarly derivable only through hindsight.

Accordingly, it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of anticipation in regard to any claim in the application but, rather, has either accorded no weight to particular explicit recitations of the

claims or is mistaken in regard to the actual content of Hummler; in some cases (e.g. claims 12 - 20) supplementing Hummler through a clearly evident exercise in impermissible hindsight. Accordingly, it is respectfully submitted that the rejection of claims 1 - 4, 7 - 12 and 14 - 20 is clearly in error and untenable.

ARGUMENT VIID. REJECTIONS UNDER 35 U.S.C. §103

A. Claims 5 and 6 based on Hummler, alone

Claims 5 and 6 depend serially from claim 1 and this ground of rejection assumes the propriety of the rejection of claim 1 under 35 U.S.C. §102 which has been demonstrated, above, to be improper. The Examiner does not assert that any of the above-described differences of claim 1 from Hummler would be obvious and, as discussed above, clearly could not properly considered to be obvious. The Examiner simply admits that use of a polysilicon hard mask to mask the first area is not disclosed by Hummler but merely states a conclusion *without indicating any compelling line of reasoning* that use of such a polysilicon hard mask to mask the first area would be obvious from disclosure of use of such a hard mask to mask a second area. Thus, no *prima facie* demonstration of obviousness has been properly made for that reason alone.

Further, Hummler discloses use of an oxide mask *in combination with an oxide liner* and then discloses that polysilicon can be used instead of the oxide layer but, evidently, still in combination with nitride. Claim 1 recites that the mask is either polysilicon *or* a combination of two materials and it is respectfully submitted that, as discussed above, Hummler does not teach use of a polysilicon hard mask alone or the derivation of the meritorious effect of step height reduction which facilitates planarization when using a polysilicon hard mask for removal of oxide and nitride as disclosed in ¶0015. Therefore, it is respectfully submitted that use of a polysilicon hard mask has not been and cannot be demonstrated to be obvious based on the scope and content of the prior art discernable from Hummler.

B. Claim 13 based on Hummler and Gustafson

Claim 13 depends from claim 12 and additionally recites performing end-point detection for termination of a non-selective etching process. In this ground of

rejection, the Examiner also assumes the propriety of the rejection of claim 12 which has been demonstrated, above, to be in error and reliant upon impermissible hindsight. The Examiner admits that Hummler does not teach end-point detection for etching and cites Gustafson for showing that end-point detection is known.

It is conceded that end-point detection for control of etching processes is known and it is respectfully submitted that Gustafson provides little of relevance to the present invention beyond that fact. Gustafson discloses a method and apparatus for etching deep trenches which must be terminated after a first through-hole is produced and indicates that known end-point detection is insufficient for that application; proposing to detect an end-point by an increase in flow of backside gas. Such a technique would be inoperable for etching of a surface. Moreover, known end-point detection techniques of the sort Gustafson may be indicating to be insufficient for deep trench etching often rely on detection of a particular reaction product or by-product. For this reason, it is respectfully submitted that end-point detection by known techniques would be counter-intuitive for non-selective etching processes (which neither Hummler nor Gustafson teaches or suggests, as discussed above) where many different reaction products may be concurrently generated. Accordingly, it is respectfully submitted that the Examiner has not made and cannot make a *prima facie* demonstration of obviousness of the subject matter of claim 13, including the subject matter of claim 12.

ARGUMENT VIIE. REJECTION OTHER THAN 35 U.S.C. §§102, 103 AND 112

There are no grounds of rejection other than under 35 U.S.C. §§102 and 103.

VIII. CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. A method for manufacture of an integrated circuit having structures formed in respective first and second areas thereon, said method comprising steps of

reducing height of structures in said first and second areas to control step height in said first and second areas,

removing a material from said first and second areas simultaneously or sequentially, and replacing said material removed from said first and second areas with a first material in said first area and a second material in said second area, respectively, one of said first and second materials being an isolation material,

using a polysilicon block-out mask or a block-out mask having two layers of different materials to protect one of said first and second areas to separately process the other of said first and second areas,

planarizing said first and second materials to provide a planar surface, and

completing said integrated circuit.

2. The method as recited in claim 1, wherein said isolation material is an array top oxide.

3. The method as recited in claim 1, wherein a polysilicon hard mask is used to mask said second area.

4. The method as recited in claim 3, wherein said polysilicon hard mask comprises a single layer of polysilicon.

5. The method as recited in claim 1, wherein a polysilicon hard mask is used to mask said first area.

6. The method as recited in claim 5, wherein said polysilicon hard mask comprises a single layer of polysilicon.

7. The method as recited in claim 1, including the further step of depositing a nitride liner prior to said step of depositing said isolation material.

8. The method as recited in claim 1, including the further step of

equalizing heights of structures in said first and second areas by etching prior to said planarizing step.

9. The method as recited in claim 1, wherein said integrated circuit is a memory device, said first area is a memory array area and said second area is a support area.

10. The method as recited in claim 1, wherein said integrated circuit includes an embedded memory, said first area is a memory array area and said second area is a support area.

11. The method as recited in claim 1, wherein said planarizing step includes

applying a planarizing material over said structures in said first and second areas and said first and second materials, and

non-selectively etching said planarizing material, said first material, said second material and said structures.

12. A method for planarizing a surface having structures formed thereon and an additional layer of material covering said surface and said structures formed on said surface, said method including steps of

applying a planarizing material to said additional layer of material to form a substantially planar surface above said surface having structures formed thereon, and

performing a non-selective etching from said substantially planar surface to a said structure formed thereon.

13. The method as recited in claim 12, including the further step of

performing end point detection to detect a material interface for determining termination of said step of non-selective etching.

14. A method as recited in claim 12, wherein

said structures have a first average height in a first area of said surface and structures of a second average height greater than said first average height in a second area of said surface, said method comprising the further steps of

etching said structures of said second average height to an average height substantially equal to said first average height,

subsequent to said etching step, applying a planarizing material to said first and second areas of said surface and covering said structures remaining in said first and second areas whereby a surface of said planarizing material is substantially planar, and

performing said step of non-selectively etching said planarizing material and structures overlaid by said planarizing material to completely remove said planarizing material and form a planar surface.

15. The method as recited in claim 12, wherein said step of non-selective etching includes removal of a nitride liner below said layer of material.

16. A method for planarizing a surface of a body of material, said method including steps of

applying a planarizing material to said body of material to form a substantially planar surface, and

performing a non-selective etching from said substantially planar surface to a point on or within said body of material.

17. The method as recited in claim 16 in combination with a top oxide early process for forming an integrated circuit.

18. The method as recited in claim 16 in combination with a top oxide nitride process for forming an integrated circuit.

19. The method as recited in claim 16 in combination with a top oxide late process for forming an integrated circuit.

20. The method as recited in claim 16 including the further step of adjusting height of a structure on a differentiated area of said body of material.

IX. Evidence Appendix

No additional evidence is relied upon in this Appeal.

X. RELATED PROCEEDINGS APPENDIX

There are no related proceedings involved in this Appeal.

Conclusion

For the reasons discussed above, it is respectfully submitted that the Examiner has not made a *prima facie* demonstration of anticipation of any claim in the application and has improperly rejected claims while effectively ignoring explicit recitations of the claims (e.g. by according them no patentable weight) or by construing Hummler well beyond the actual content thereof; often effectively supplementing the content of Hummler through hindsight in light of the present disclosure. The deficiencies of Hummler are not mitigated by the level of ordinary skill in the art discernible from Hummler or the teachings of Gustafson. Accordingly, it is respectfully submitted that all grounds of rejection asserted by the Examiner are clearly untenable and reversal of the Examiner is respectfully requested.

Respectfully submitted,

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis, Christofferson & Cook, P.C.
11491 Sunset Hills Road, Suite 340
Reston, VA 20190
Tel. (703) 787-9400
Fax. (703) 787-7557
Customer No. 30743